

FIG. 1

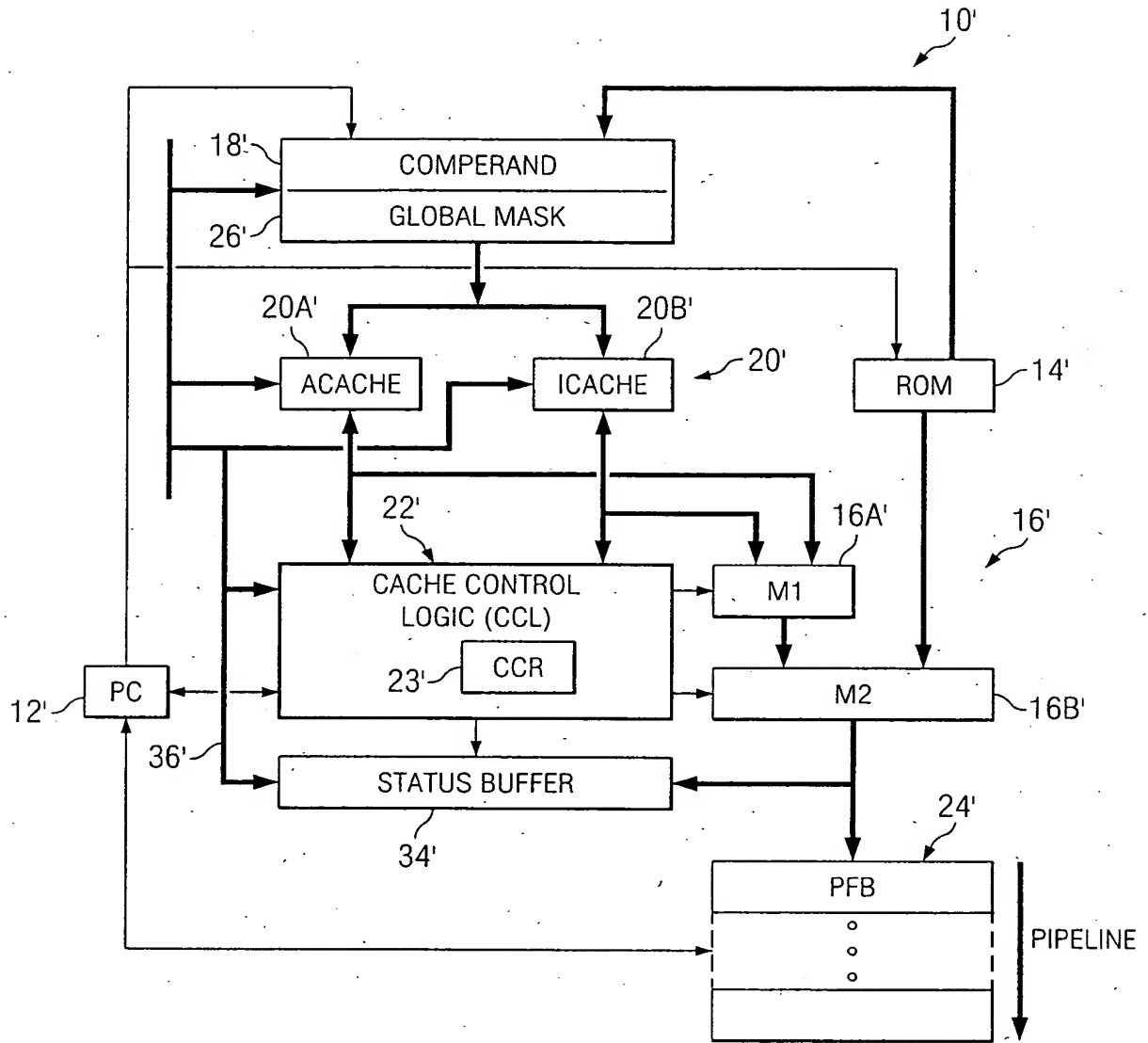


FIG. 2

CONTROL FLAGS	FIELD	OPERATION	OTHER	EXPLANATION
1.	V			VALID
2.	A			ADDRESS
3.	O			OPCODE
4.	G			GLOBAL
5.		I		INSERT
6.		M		MATCH
7.		B		BLOCK ASSIGNMENT
8.		X		DELETE
9.			E	EXTERNAL ROM
10.			H	HALT
11.			L	LOCK
12.			Q	GENERATE TRAP

FIG. 3

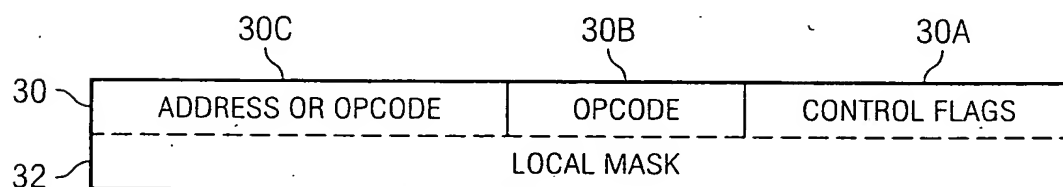


FIG. 4

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
DM	PI	SM	SI	ICE	II										SA	IA										ACE	ICL	ACL	OF			

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FIELD	DEFINITION	EXPLANATION
OF(0)	ENABLE OPERATION FLAG	ENABLE FULL CACHE OPERATION (ENABLED=1, DEFAULT=0)
ACL(1)	ACACHE LOCK	PREVENTS WRITE INTO ACACHE LINES (ENABLED=1, DEFAULT=0)
ICL(2)	ICACHE LOCK	PREVENTS WRITE INTO ICACHE LINES (ENABLED=1, DEFAULT=0)
ACE(3)	ACACHE ENABLE	TURNS ON THE ADDRESS CACHE BLOCK (ENABLED=1, DEFAULT=0)
IA(14:4)	ACACHE LINE INDEX	INDEX OF ACACHE LINE MATCHING COMPERAND
SA (15)	ACACHE MATCH STATUS	REPORT MATCH STATUS (VALID=1, NO MATCH=0)
II(26:16)	ICACHE LINE INDEX	INDEX OF ICACHE LINE MATCHING COMPERAND
ICE(17)	ICACHE ENABLE	TURNS ON INSTRUCTION CACHE CIRCUIT BLOCK
SI(28)	ICACHE MATCH STATUS	REPORT MATCH STATUS FOR ICACHE (0=NO MATCH, 1=MATCH)
SM(29)	SELF-MODIFY	ENABLES ROM CODE TO MODIFY A/CACHE (ENABLED=1, DEFAULT=0)
PI(30)	PRIORITY INDICATOR	ESTABLISHES PRIORITY OF DUAL MATCH RESULTS (0= ACACHE, 1=ICACHE)
DM(31)	DEBUG MODE	DUMP CACHE LINE MATCHES TO BUFFER RATHER THAN INTO PIPELINE

FIG. 5